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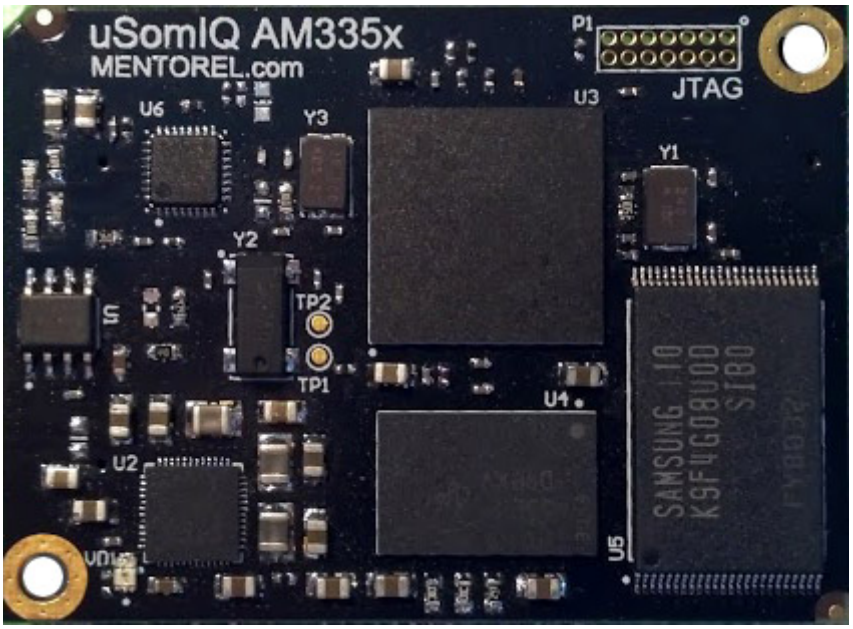

uSomIQ AM335x

System-On-Module

Technical Reference Manual

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DIAGRAMS

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General information

1.1 About this document

This manual describes a product of the MENTOREL company. The manual specifies the uSomIQ-AM335x's design and function. Precise specifications for the Texas Instruments AM335x microcontrollers can be found in Texas Instrument's AM335x Data Sheet and Technical Reference Manual. This Document is subject to change without notice as we will work to keep improving the design as the product matures based on feedback and experience.

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2 Introduction

uSomIQ is a new system on module produced by MENTOREL. It features robust design and basically intended for industrial applications. It was designed to withstand extreme temperature floating and has been tested in a temperature chamber. uSomIQ mates with carrier boards by the high density mezzanine connectors FCI MezzoStak intended for extreme operating temperature range between -40 and 125 degrees C. Stub-less contact design supports PCEeG2 High Speed performance and ensures reliable operation of high-speed interfaces on the uSomIQ module: USB 2.0 and Ethernet.

2.1 Functional diagram

The following units are installed at the uSomIQ module:

- Power controller (PMIC) TPS65217C
- LDO TL5209DR for Ethernet PHY
- MPU AM335x
- DDR3 memory
- SLC NAND
- Ethernet PHY SMSC (Microchip) LAN8710

Diagram 1 shows the main module units.

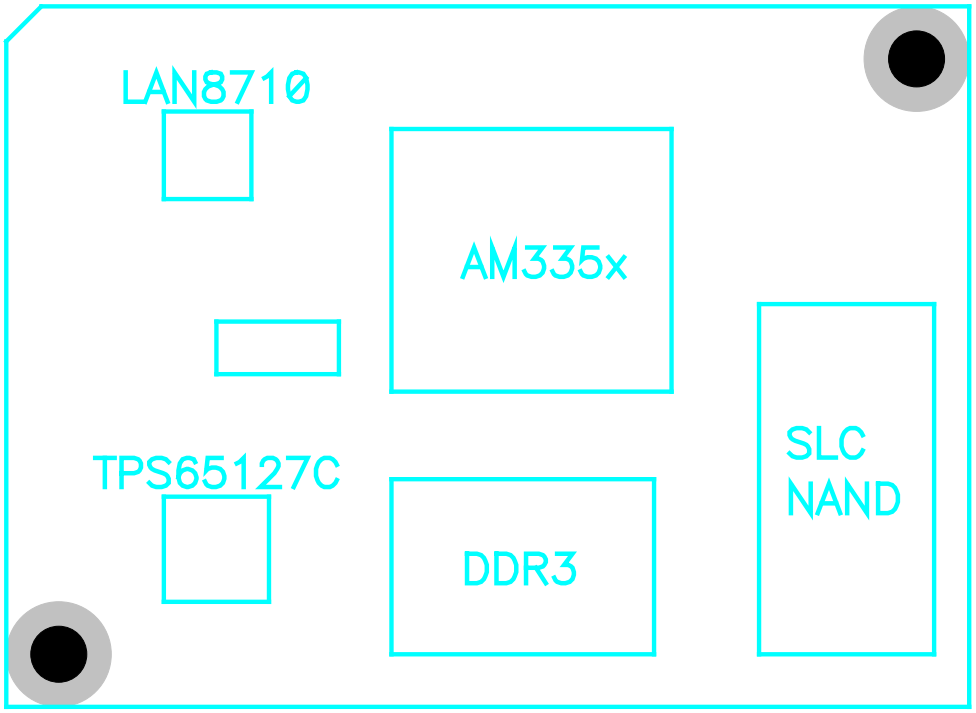

Diagram 1. uSomIQ block diagram.

2.1 Main features

The following features are common for the uSomIQ family:

- DDR3 or DDR3L SDRAM: **128MB – 1024MB**
- SLC NAND Flash: **128MB – 4GB**
- LCD Up to 24-Bit Data Output; 8 Bits per Pixel (RGB)
- Resolution up to 2048 x 2048 (with Maximum 126-MHz Pixel Clock)
- High Speed (480Mbit) USB 2.0 OTG (Host/Device)
- High Speed (480Mbit) USB 2.0 Host

- 12-Bit Successive Approximation Register (SAR) ADC
- Up to Two Controller-Area Network (CAN) Ports (Supports CAN Version 2 Parts A and B)
- Ethernet PHY SMSC LAN8710 (MII) 10/100Mbit
- Up to five UART ports
- McASP, McSPI, I2C interfaces
- Two 8-bit SD/MMC+ ports
- Flexible 8-Bit and 16-Bit Asynchronous Module Memory Interface with up to Seven Chip Selects (NAND, NOR, Muxed-NOR, SRAM)
- Lots of General-Purpose I/O (GPIO) lines
- JTAG and cJTAG for ARM
- Unique MAC address (factory programmed to CPU)
- IO level 3.3V (fixed)
- Single power supply 5V
- Power consumption 2.5W maximum running at 1GHz
- uSomIQ dimensions (55x40mm)
- Working temperature:
    - Industrial -40..+85°C
    - Extended -20..+85°C
    - Commercial 0..+70°C (available for custom orders)

2.2 High level description

2.2.1 Sitara processors

uSomIQ utilizes Sitara family of embedded processors based on ARMv7 architecture and introduced by Texas Instruments and may hold one of the following AM335x processors in ZCZ package:

2.2.1.1 AM3358

Features:

- ARM Cortex-A8 32-Bit RISC
- ARM core frequency: 600 MHz, 800 MHz or 1000MHz
- Cache L1: I-cache 32KB and D-cache 32KB
- L2 Cache: 256KB of L2 Cache with Error Correcting
- 64KB of internal SRAM
- NEON Single Instruction MultiData (SIMD) Integer
- POWERVR SGX530 3D Graphics Engine
- Touchscreen controller upto 8 lines
- Controller Area Network (CAN)
- Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem (PRU-ICSS)

2.2.1.2 AM3354

Features:

- ARM Cortex-A8 32-Bit RISC
- ARM core frequency: 600 MHz, 800 MHz or 1000MHz

- Cache L1: I-cache 32KB and D-cache 32KB
- L2 Cache: 256KB of L2 Cache with Error Correcting
- 64KB of internal SRAM
- NEON Single Instruction MultiData (SIMD) Integer
- POWERVR SGX530 3D Graphics Engine
- Touchscreen controller upto 8 lines
- Controller Area Network (CAN)

2.2.1.3 AM3352

Features:

- ARM Cortex-A8 32-Bit RISC
- ARM core frequency: 300 MHz, 500MHz, 600 MHz, 800 MHz or 1000MHz
- Cache L1: I-cache 32KB and D-cache 32KB
- L2 Cache: 256KB of L2 Cache with Error Correcting
- 64KB of internal SRAM
- NEON Single Instruction MultiData (SIMD) Integer
- Touchscreen controller upto 8 lines
- Controller Area Network (CAN)

2.2.2 Baseboard connectors

uSomIQ AM335x requires a baseboard to carry the main power supply 5V as well as necessary interfaces connectors (Ethernet, SD, etc). uSomIQ uses two FCI MezzoStak 70-pin connectors to interface the baseboard.

The following signals and interfaces are available on the baseboard connectors:

- 5VDC input to feed the module (all necessary voltages are created by the PMIC installed)
- 3.3V output to feed external devices (an end-user design should not overload this output because it can lead to damage of the SOM)
- Hi-Speed USB OTG (host/device)
- Hi-Speed USB HOST
- LCD 16/24bit for LVDS/TTL/DVI/HDMI
- SD/MMC0, SD/MMC1, SD/MMC2
- SPI0, SPI1
- McASP0
- UART0, UART1, UART2, UART3
- GPMC 16bit data/address + 4x CS
- i2c0/i2c1/i2c3
- ADC 8-inputs
- Ethernet 10/100

- Controller Area Network (CAN)

Most of the controller pins have multiple multiplexed functions. All functions are listed in the tables 2 and 3. If a user experiences difficulties in proper configuring of necessary functions Texas Instruments has developed a Windows-based application called Pin Mux Utility that helps a system designer select the appropriate pin-multiplexing configuration for their AM335x-based product design. The Pin Mux Utility provides a way to select valid IO Sets of specific peripheral interfaces to ensure the pinmultiplexing configuration selected for a design only uses valid IO Sets supported by the AM335x device.

Please note that all module connections are not to exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller manuals/data sheets. As damage from improper connections varies according to use and application, it is the user's responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

2.2.3 Power management

PMIC TPS65217C creates all necessary voltages: 1.2V (ARM core), 1.35V/1.5V (DDR3), 1.8V (ADC reference), 3.3V (I/O). Ethernet PHY is powered by a discrete LDO TL5029 (may differ in some configurations).

2.2.4 USB 2.0 OTG

The MPU's port USB0 can function as USB OTG.

This device implements the USB2.0 OTG dual port module and PHY for interfacing to USB as a peripheral or host. A Mode of operation is identified by a state of the USB_ID line. Supports USB 2.0 host or OTG at speeds HS (480 Mb/s), FS (12 Mb/s), and LS (1.5 Mb/s). Supports USB 2.0 peripheral at speeds HS (480 Mb/s) and FS (12 Mb/s).

USB OTG port can function as:

- USB ACM (serial interface)
- USB Ethernet
- MPU boot

2.2.5 USB 2.0 Host Port

The MPU's port USB1 can function only in USB Host mode, because the USB1_ID pin is grounded on the module.

Supports USB 2.0 host at speeds HS (480 Mb/s), FS (12 Mb/s), and LS (1.5 Mb/s). All low-speed devices like a mouse or a keyboard can be connected directly to this port.

2.2.6 LCD interface

This interface is for connection of industrial and other TFT panels. In addition LVDS or DVI-D/HDMI serializers can be connected to achieve true-color palette 24-bits (8b RGB).

2.2.7 SD/MMC

MMC0, MMC1 and MMC2 interfaces are available on the baseboard connectors. MMC1 and MMC2 is multiplexed with the GPMC bus. Improper configuration of MMC1/2 interfaces will break the NAND functionality.

MMC0 and MMC1 accepts only 3.3V voltage level.

MMC command/response sets as defined in the MMC standard specification v4.3.
SD command/response sets as defined in the SD Physical Layer specification v2.00

It is possible to implement eMMC boot by placing an eMMC IC onto a baseboard. Proper pinmux configuration is required as well modifications to the default BSP.

2.2.8 LED

LED marked as VD1 is connected to PMIC TPS65217C. It lights up when PMIC works properly and 5VDC is applied to the module. If any problem with power is detected this LED blinks or stays blank.

2.2.9 JTAG

12-pin connector exists on the module for JTAG functionality. The JTAG interface accepts 3.3V levels only. Please ensure your JTAG emulator is compatible with this requirement.

3 uSomIQ Architecture

This section provides the detailed specification of uSomIQ.

3.1 Functional Diagram

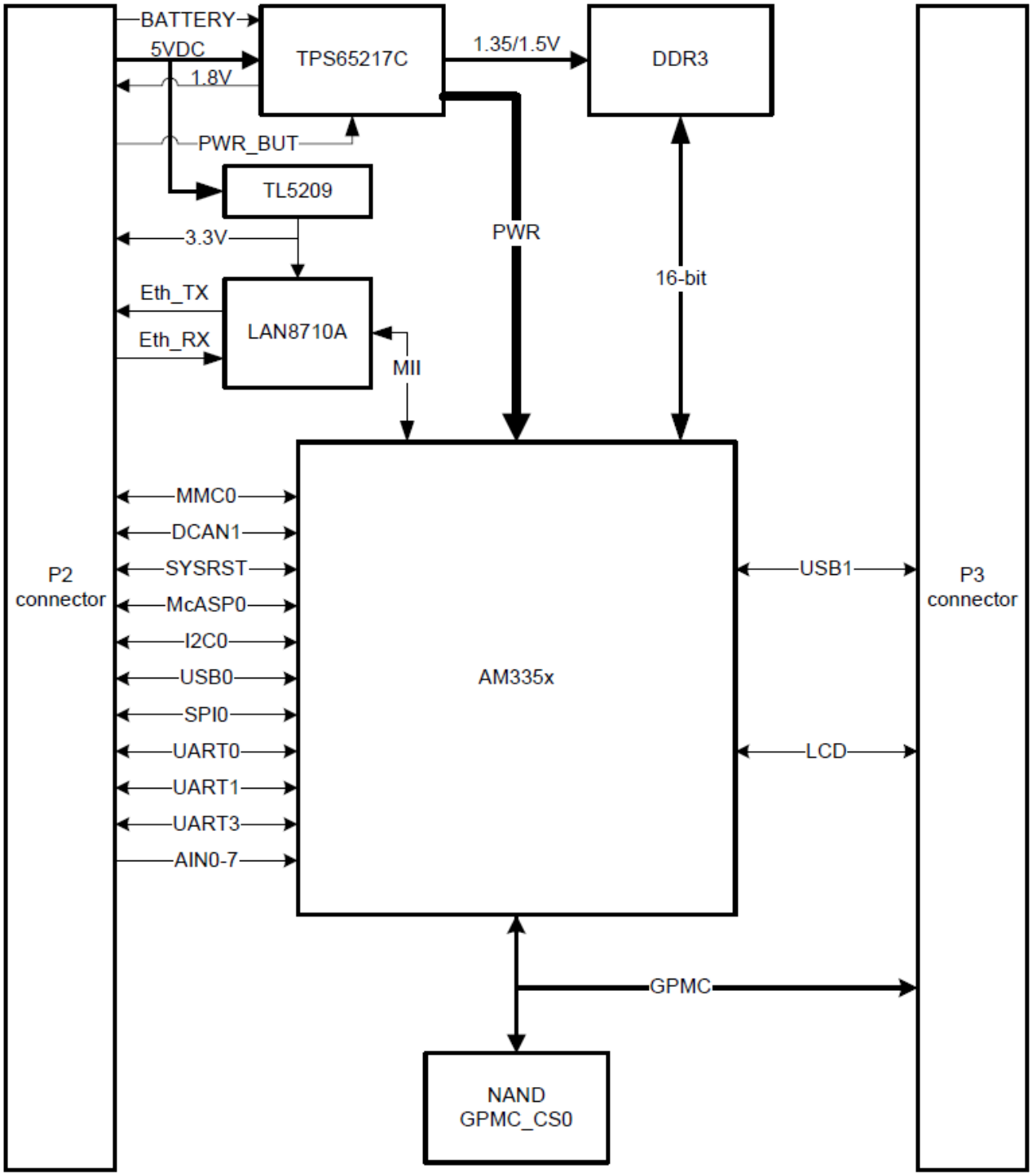

Diagram 2. uSomIQ Functional Diagram.

3.2 AM335x microprocessor

AM335x MPU is the main unit on the uSomIQ module. Diagram 3 shows maximum capabilities introduced by AM335x family.

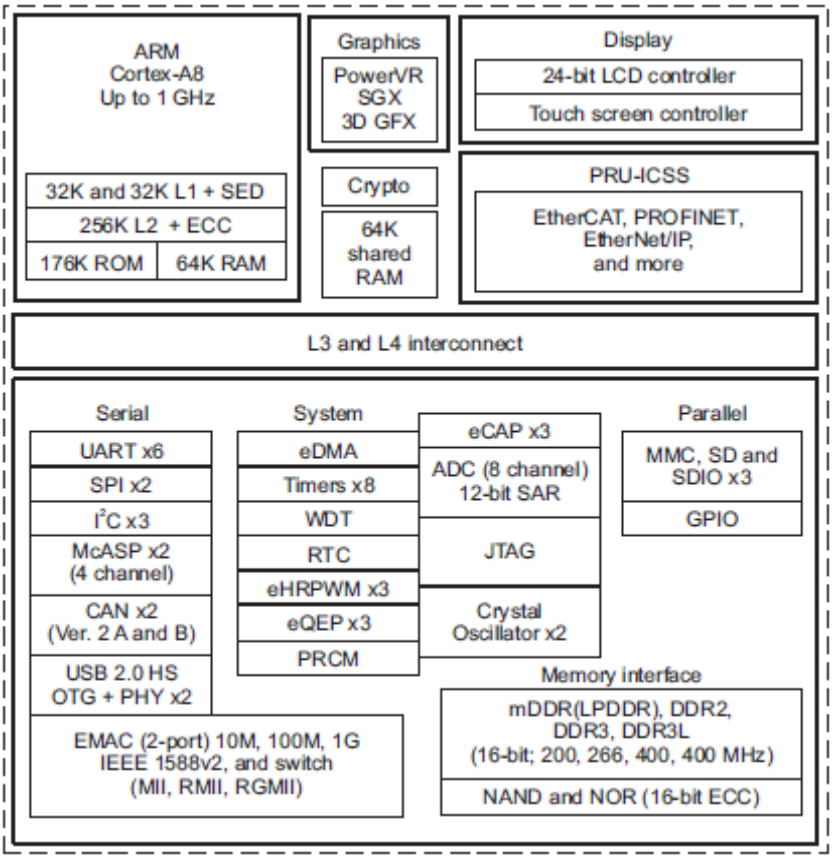

Diagram 3. AM335x Functional Block Diagram.

The AM335x microprocessors, based on the ARM Cortex-A8, are enhanced with image, graphics processing, peripherals and industrial interface options such as EtherCAT and PROFIBUS. The device supports the following high-level operating systems that are available free of charge from TI:
• Linux®
• Android™

The AM335x microprocessor contains these subsystems:

- Microprocessor unit (MPU) subsystem based on the ARM Cortex-A8 microprocessor.
- POWERVR SGX™ Graphics Accelerator subsystem for 3D graphics acceleration to support display and gaming effects.
- The Programmable Real-Time Unit and Industrial Communication Subsystem (PRU-ICSS) is separate from the ARM core, allowing independent operation and clocking for greater efficiency and flexibility.
- The PRU-ICSS enables additional peripheral interfaces and real-time protocols such as EtherCAT, PROFINET, EtherNet/IP, PROFIBUS, Ethernet Powerlink, Sercos, and others.
- External Memory Interfaces EMIF – 400MHz DDR3 SDRAM
- General-Purpose Memory Controller GPMC – Flexible 8-Bit and 16-Bit Asynchronous memory interfaces for NAND, NOR, SRAM
- LCD controller
- SD/MMC
- USB OTG
- Power management

- UART
- I2C
- McASP for Audio (I2S)
- JTAG
- Controller Area Network (CAN)

The module can carry any processor from AM335x Sitara family in ZCZ package. uSomIQ accepts any processor with running frequency from 275MHz to 1GHz.

3.3 Memory

Described in the following sections are the three memory devices found on the board.

3.3.1 DDR3

uSomIQ is designed to carry DDR3 or DDR3L memory with any amount of 128MB to 512MB. The maximum amount is achieved by using a single 256Mb x16 DDR3L 4Gb (512MB) memory device. The memory used is the MT41K256M16HA-125 from Micron. It will operate at a clock frequency of 400MHz yielding an effective rate of 800MHZ on the DDR3L bus allowing for 1.6GB/S of DDR3L memory bandwidth.

In order to provide necessary working temperature proper part numbers are used.

3.3.2 EEPROM

A single 4KB EEPROM is provided on I2C0 that holds the board information. This information includes board name, serial number, and revision information. uSomIQ identifier is “AM335USOM”. This value is preloaded during manufacturing.

Note: some configurations may not have this EEPROM due to expense purposes if a customer demands it.

3.3.3 NAND

A single 128MB - 4GB SLC NAND device is on the board. The device connects to the GPMC bus of the processor, allowing for 8bit wide access (can be also configured for 16bit NAND devices). Default boot mode for the board will be NAND first with an option to change it to MMC0, the SD card slot, for booting from the SD card as a result of removing and reapplying the power to the board. Simply pressing the reset button will not change the boot mode.

3.4 Power Management

3.4.1 The main power source requirements

To feed the SOM with the power you need to supply the stabilized voltage. The following requirements are for the main power source:

- Voltage level: 4.3-5.5 VDC
- Current: 300-1000 mA

It is recommended to install a Low-ESR capacitor close to 5VDC pins of the respective baseboard connector.

3.4.2 Onboard power sources

The PMIC TPS65217C creates all voltage levels necessary for proper functionality of DDR3 and MPU. In addition to TPS65217C a LDO TL5209 is used to create 3.3Vto feed the Ethernet PHY.

The TL5209 IC forms 3.3V from the main voltage supplied to the SOM. It provide current up to 500mA and feeds the Ethernet PHY. 3.3V output from TL5209 is available on a baseboard connector. It can be used to feed any external circuit with maximum power consumption 400mA.

3.4.3 Main power rails

The PMIC TPS65217C provides three main power rails used by AM335x and peripherals:

- VDDS_DDR (1.35 or 1.5V)
- VDD_MPU (1.1V)
- VDD_CORE (1.1V)

These three voltages are created by impulse DC/DC convertors. Other voltages used by peripherals are created by internal LDOs on the TPS65217C:

- LDO3 (1.8V)
- LDO4 (3.3V)
- VLDO1 (3.3V)
- VLDO2 (3.3V)

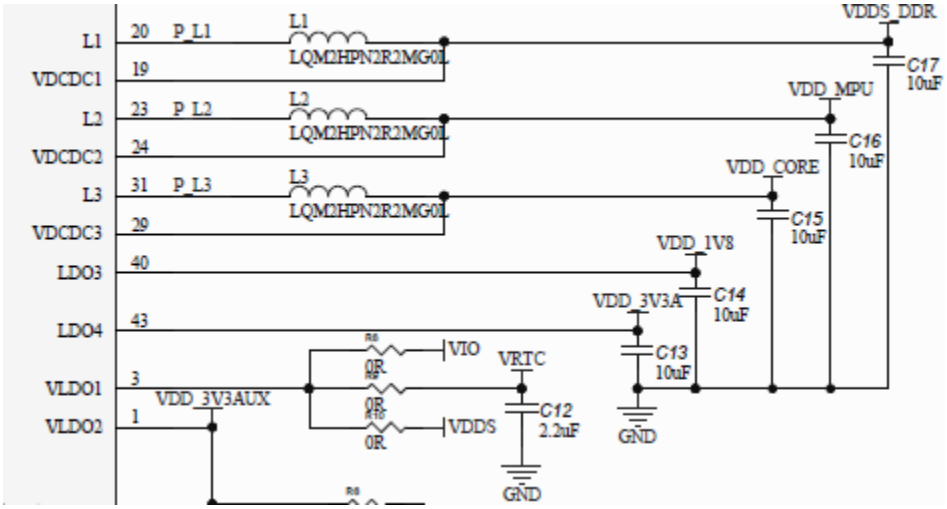

Diagram 4. Main power rails.

3.4.4 CPU control over TPS65217C

The PMIC TPS65217C is controlled by a CPU with I2C bus. I2C0 bus is in the connection between the TPS65217C and the CPU. A designer should limit the use of the I2C0 bus because it can, but not necessarily, disturb the power management.

3.5 External memory interface EMIF

The EMIF interface is used to bear DDR3 memory with 16-bit wide bus. CS0 signal is used for DDR3 addressing.

DDR3 SDRAM CS0 base address: 0x8000 0000

Space addressed: 0x8000 0000 – 0xBFFF FFFF

Memory size is specified during the bootstrap u-boot loading. The first level loader SPL initializes the SDRAM and loads there u-boot.

3.6 GPMC

3.6.1 NAND

NAND flash can be used for using uSomIQ without external memory devices like SD/MMC. NAND flash for the module booting is on GPMC_CS0 line. Usually only 8-bit devices are used with uSomIQ but for custom orders NAND ICs can be changed to 16-bit ones. In addition to CS0 and DATAxx lines two more signals are utilized:

- GPMC_WAIT0 – ready/busy
- GPMC_NWP – write protect

Possible part number for the NAND flash installed on the module is Micron MT29F4G08ABADAWP

3.6.2 Other devices on GPMC

The GPMC bus is routed to the onboard P3 connector, including chip-select signals (CS): CS0, CS1, CS2, CS3.

Warning: **GPMC_NBE0_CLE signal is used for NAND flash and cannot be shared for different functions.**

The general-purpose memory controller (GPMC) is a unified memory controller dedicated to interfacing external memory devices:

- Asynchronous SRAM-like memories and application-specific integrated circuit (ASIC) devices
- Asynchronous, synchronous, and page mode (only available in non-multiplexed mode) burst NOR flash devices
- NAND Flash
- Pseudo-SRAM devices

3.7 LCD controller

The LCD controller consists of two independent controllers, the Raster Controller and the LCD Interface Display Driver (LIDD) controller. Each controller operates independently from the other and only one of them is active at any given time.

- The Raster Controller handles the synchronous LCD interface. It provides timing and data for constant graphics refresh to a passive display. It supports a wide variety of monochrome and full-color display types and sizes by use of programmable timing controls, a built-in palette, and a gray-scale/serializer. Graphics data is processed and stored in frame buffers. A frame buffer is a contiguous memory block in the system. A built-in DMA engine supplies the graphics data to the Raster engine which, in turn, outputs to the external LCD device.
- The LIDD Controller supports the asynchronous LCD interface. It provides full-timing programmability of control signals (CS, WE, OE, ALE) and output data.

3.8 Touchscreen Controller

The touchscreen controller and analog-to-digital converter subsystem (TSC_ADC_SS) is an 8-channel general-purpose analog-to-digital converter (ADC) with optional support for interleaving touchscreen (TS) conversions for a 4-wire, 5-wire, or 8-wire resistive panel. The TSC_ADC_SS can be configured for use in one of the following applications:

- 8 general-purpose ADC channels
- 4-wire TSC with 4 general-purpose ADC channels
- 5-wire TSC with 3 general-purpose ADC channels
- 8-wire TSC

3.9 Multichannel Audio Serial Port (McASP)

The multichannel audio serial port (McASP) functions as a general-purpose audio serial port optimized for the needs of multichannel audio applications. The McASP is useful for time-division multiplexed (TDM) stream, Inter-Integrated Sound (I2S) protocols, and intercomponent digital audio interface transmission (DIT). The McASP consists of transmit and receive sections that may operate synchronized, or completely independently with separate master clocks, bit clocks, and frame syncs, and using different transmit modes with different bit-stream formats. The McASP module also includes serializers that can be individually enabled to either transmit or receive.

3.10 USB

The USB controller provides a low-cost connectivity solution for numerous consumer portable devices by providing a mechanism for data transfer between USB devices with a line/bus speed up to 480 Mbps. The device USB subsystem has two independent USB 2.0 Modules built around two OTG controllers. The OTG supplement feature, the support for a dynamic role change, is also supported. Each port has the support for a dual-role feature allowing for additional versatility enabling operation capability as a host or peripheral. Both ports have identical capabilities and operate independent of each other. Diagram 4 shows the USB subsystem:

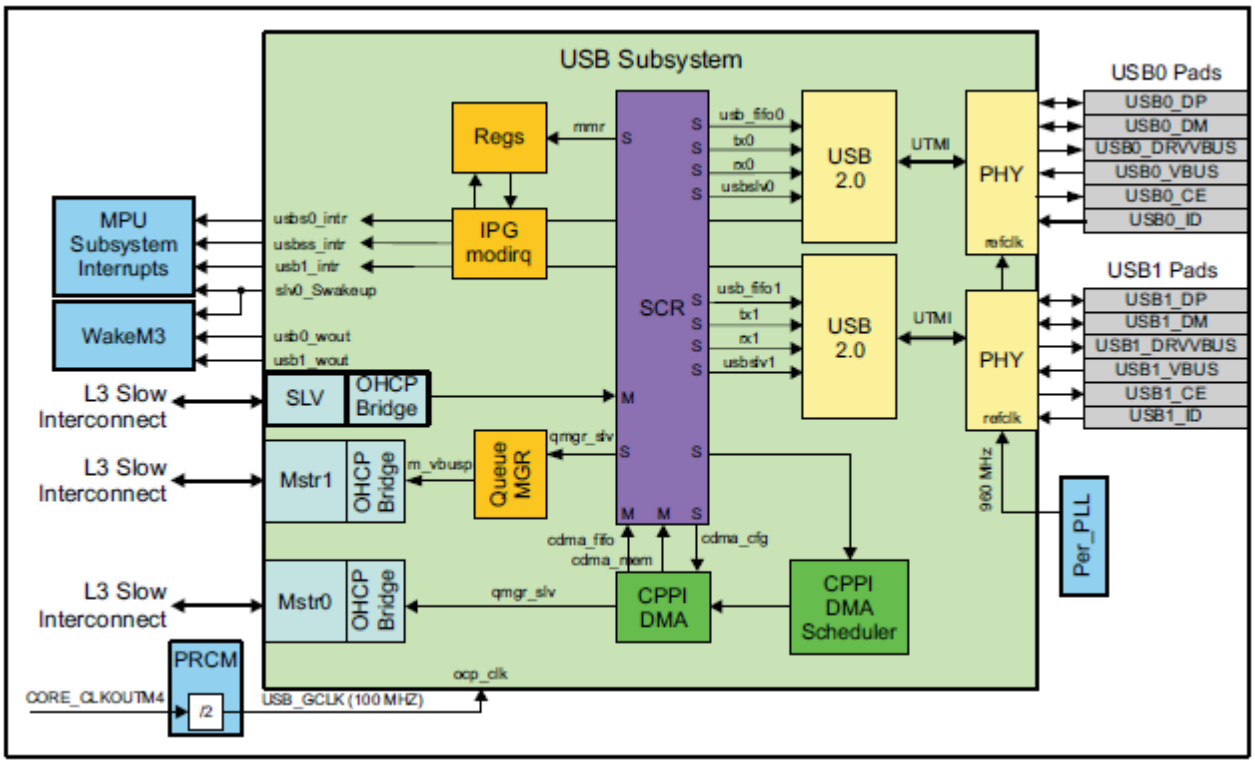

Diagram 5. USB subsystem block diagram.

However in the uSomIQ design USB1 port acts always in Host mode while USB0 supports host, device and OTG features (USB0_ID is floating).

3.10.1 USB0 - OTG port

The USB0 interface of the processor is configured to work in OTG-mode. The USB0_ID line is routed to a baseboard connector allowing an end-system designer to configure this port in Device-, Host- or OTG mode. Setting USB0 mode is done by pulling USB0_ID line to Ground (Host mode) or leaving floating (Device/OTG mode).

Diagram 5 shows the USB0 connection in schematic.

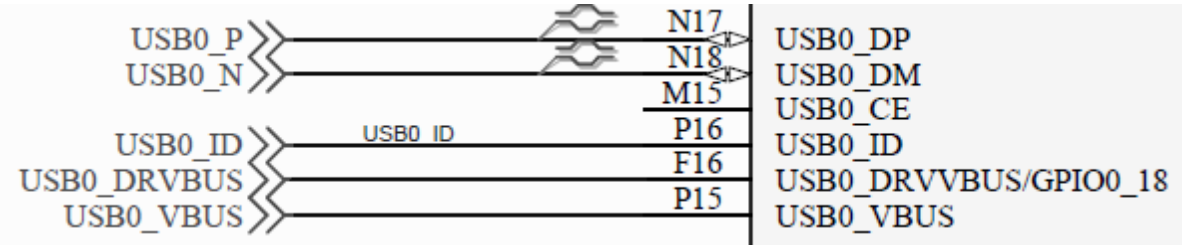

Diagram 6. USB0 signals (OTG mode).

3.10.2 USB1 - host port

The USB1 interface of the processor is configured for the Host-mode only by pulling-low the USB1_ID line in the schematic. USB1 is USB 2.0 compatible and allows direct connection of Low- and Full- speed devices like mouses or keyboards without a USB-hub.

Diagram 6 shows the USB1 connection in schematic.

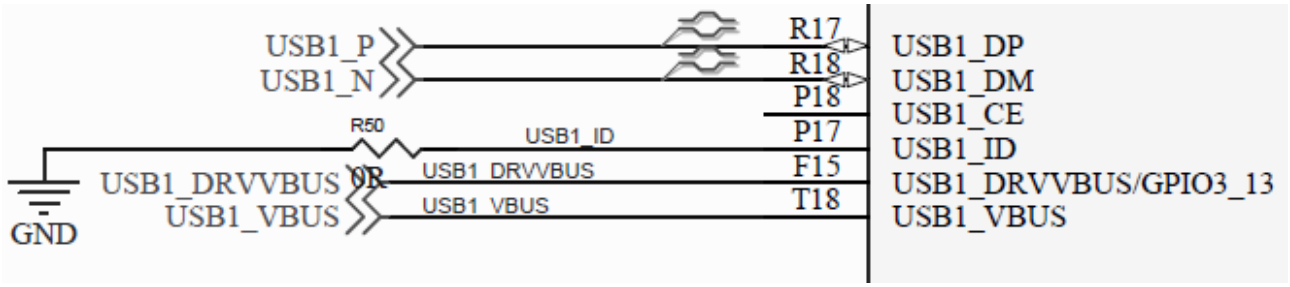

Diagram 7. USB1 signals (Host mode).

3.11 SD/MMC

This device contains three instances of the Multimedia Card (MMC), Secure Digital (SD), and Secure Digital I/O (SDIO) high speed interface module (MMCHS). The controller provides an interface to an MMC, SD memory card or SDIO card.

uSomIQ introduces three interfaces: MMC0, MMC1 and MMC2. All these interfaces are multiplexed with other CPU pins. Refer to Tables 2 and 3 for details. You can use these interfaces to connect memory cards or devices wirking in SDIO mode. Interrfaces are capable to work in 4- or 8- bits mode.

3.11.1 SD/MMC card booting

The CPU Boot ROM supports SD card memory boot with the following limitations:

- MMC/SD cards compatible with Multimedia Card System Specification v4.3 or Secure Digital I/O Card Specification v2.0, including high density cards SDHC and HC MMC.
- SD/MMC cards connected to MMC0
- Cards are powered by 3.3V
- 1-bit for MMC or 4-bit for SD
- Frequency:
  - identification mode: 400 kHz
  - data transfer mode: 10MHz
- Only one card resides on the bus
- FAT12/16/32, with MBR or without

eMMC/eSD ICs can be connected to MMC1 interface only (MMC1 is multiplexed with GPMC).

3.11.2 SD/MMC connection for booting

By default uSomIQ boot pins are configured for NAND booting but an alternative way to boot a CPU is a SD or Micro-SD connection. Diagram 7 shows a proper micro-SD connection schematic to uSomIQ.

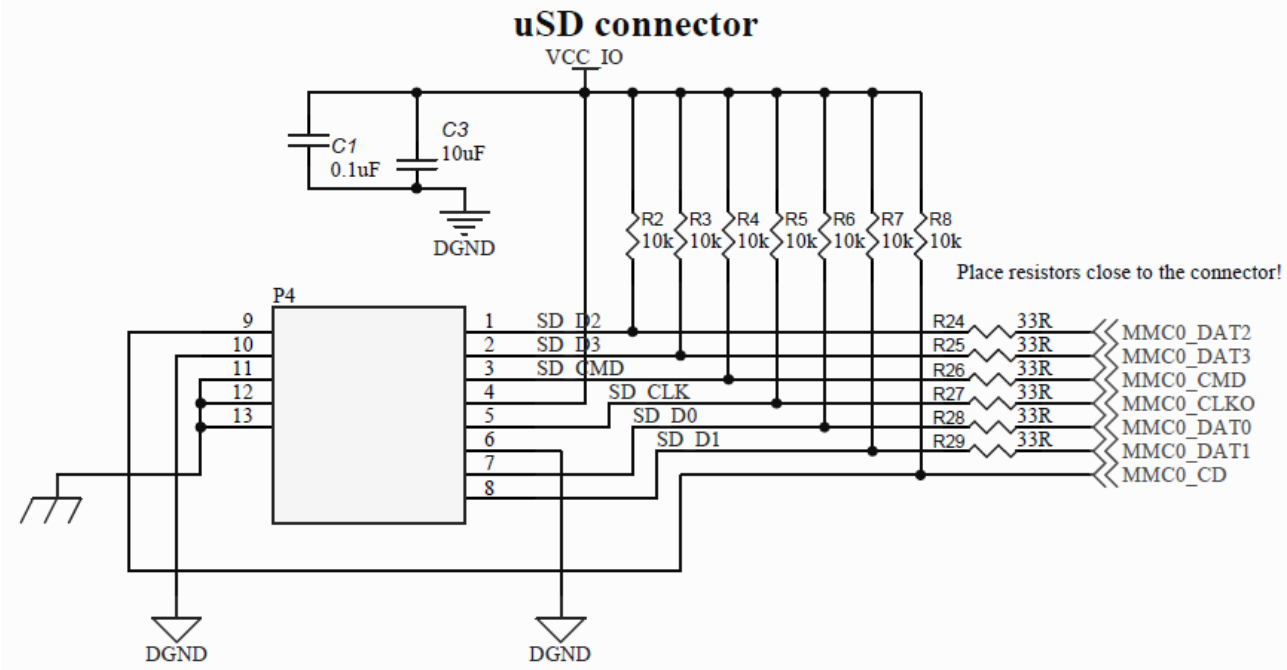

Diagram 8. SD/MMC0 connection for booting.

3.12 Controller Area Network

3.12.1 DCAN Features

The general features of the DCAN controller are:
• Supports CAN protocol version 2.0 part A, B (ISO 11898-1)
• Bit rates up to 1 MBit/s
• Dual clock source
• 16, 32, 64 or 128 message objects (instantiated as 64 on this device)
• Individual identifier mask for each message object

- Programmable FIFO mode for message objects
- Programmable loop-back modes for self-test operation
- Suspend mode for debug support
- Software module reset
- Automatic bus on after Bus-Off state by a programmable 32-bit timer
- Message RAM parity check mechanism
- Direct access to Message RAM during test mode
- CAN Rx / Tx pins configurable as general purpose IO pins
- Two interrupt lines (plus additional parity-error interrupt line)
- RAM initialization
- DMA support

3.12.2 Unsupported DCAN Features

The DCAN module in this device does not support GPIO pin mode. All GPIO functionality is mapped through the GPIO modules and muxed at the pins. GPIO pin control signals from the DCAN modules are not connected.

3.12.3 Integration

The Controller Area Network is a serial communications protocol which efficiently supports distributed realtime control with a high level of security. The DCAN module supports bitrates up to 1 Mbit/s and is compliant to the CAN 2.0B protocol specification. The core IP within DCAN is provided by Bosch.
This device includes two instantiations of the DCAN controller: DCAN0 and DCAN1.
Figure 9 shows the DCAN module integration.

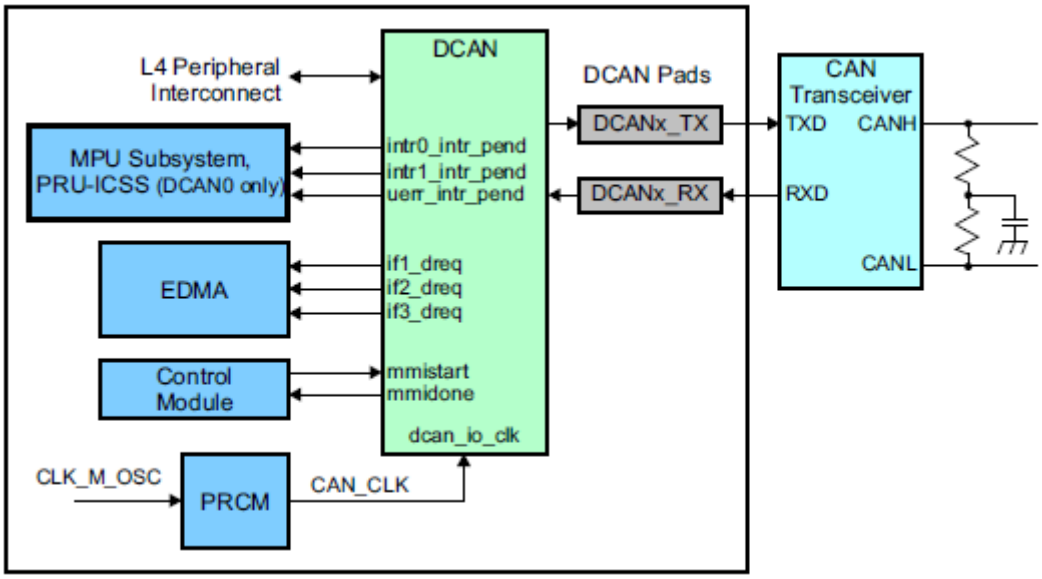

Diagram 9. DCAN Integration.

3.13 PRU-ICSS

The PRU-ICSS module is located inside the AM335x processor. Access to these pins is provided by the expansion headers and is multiplexed with other functions on the board. Access is not provided to all of the available pins.
All documentation is located at http://github.com/beagleboard/am335x_pru_package. This feature is not supported by Texas Instruments.

3.13.1 PRU-ICSS Features

The features of the PRU-ICSS include:
Two independent programmable real-time (PRU) cores:
– 32-Bit Load/Store RISC architecture
– 8K Byte instruction RAM (2K instructions) per core
– 8K Bytes data RAM per core
– 12K Bytes shared RAM
• Operating frequency of 200 MHz
• PRU operation is little endian similar to ARM processor
• All memories within PRU-ICSS support parity
• Includes Interrupt Controller for system event handling
• Fast I/O interface
– 16 input pins and 16 output pins per PRU core. (Not all of these are accessible due to reserved functions).

3.13.2 PRU-ICSS Block Diagram

Diagram 10 is a high level block diagram of the PRU-ICSS.

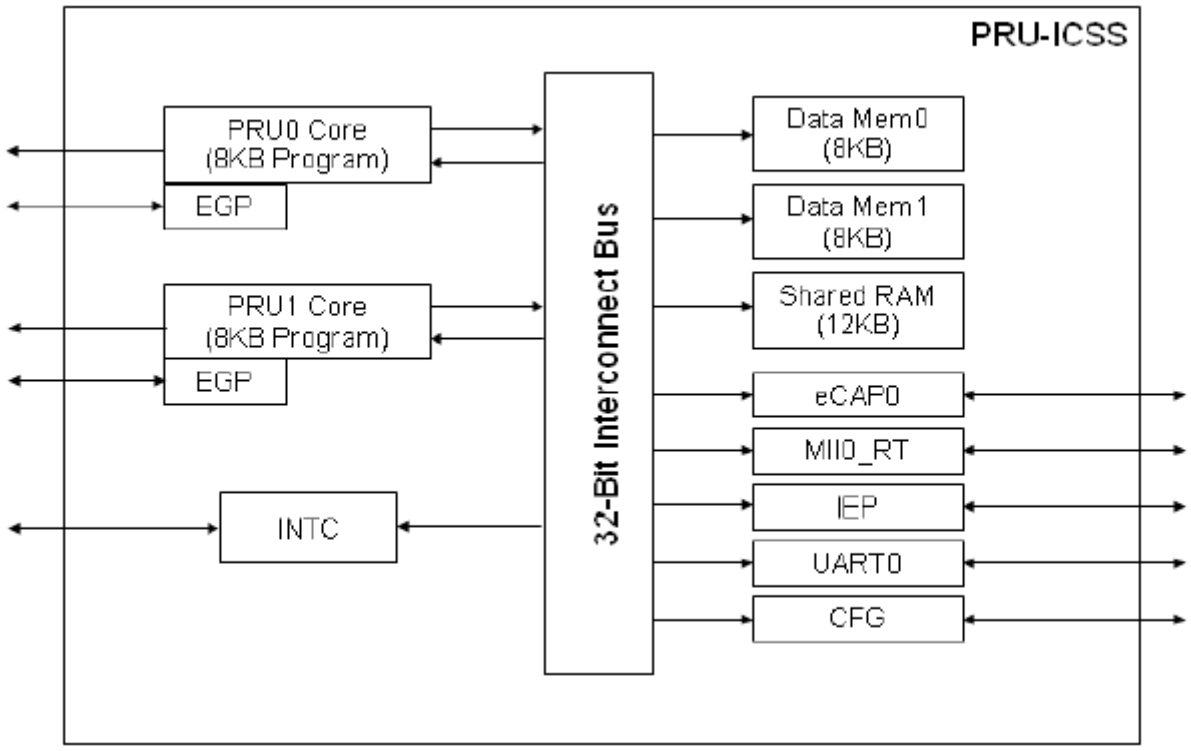

Diagram 10. PRU-ICSS Block Diagram.

3.12 JTAG

A place for an optional 14 pin CTI JTAG header is provided on the board to facilitate the SW development and debugging of the board by using various JTAG emulators. This header is not supplied standard on the board. To use this, a connector will need to be soldered onto the board. The onboard header does not have a standard pin arrangement, because of the very compact design of uSomIQ. However it has all necessary pins to be compatible to any ARM JTAG emulator. A simple wire adapter can be made between the uSomIQ JTAG header and a JTAG emulator. uSomIQ JTAG header has a footprint of the 2-row pin header with pin spacing 1.27mm. A standard TI's tool like XDS100V2 can be used to debug AM335x processor installed on uSomIQ. Diagram 8 shows how JTAG signals are arranged on the pin header.

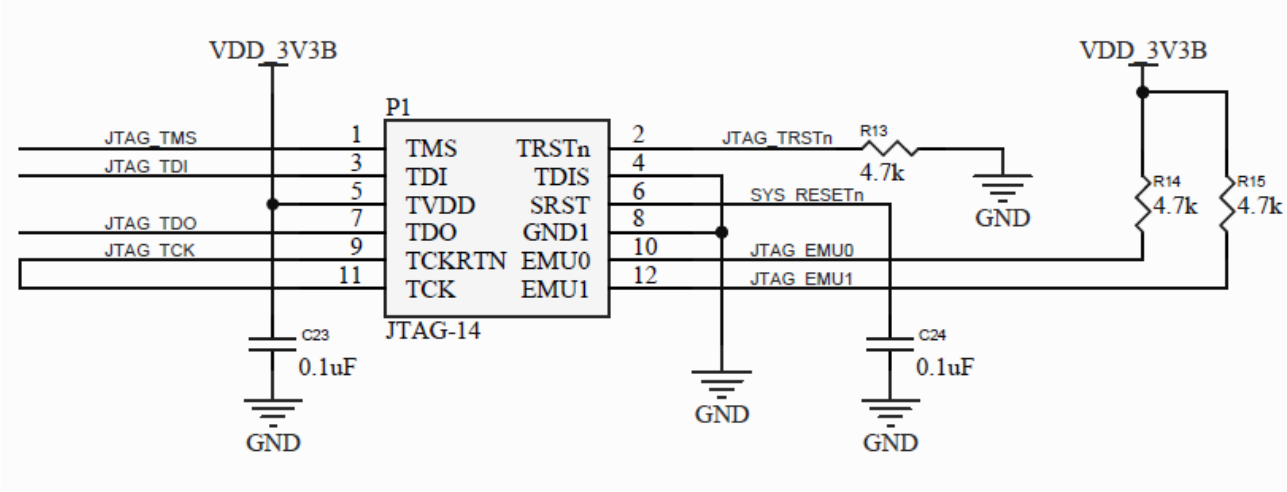

Diagram 11. uSomIQ JTAG header.

uSomIQ JTAG interface works with 3.3V emulators. Use a proper JTAG emulator.

3.13 AM335x reset

There is the single global reset signal issued by a processor or issued to the processor – SYS_RESETn. This line has an on module pull-up resistor 10 kOhm to a system 3.3V power rail. To issue a reset to the processor it is necessary to ground this signal for at least 100us. The SYS_RESETn is in fact the signal WARMRESET and therefore issuing this signal does not lead to the hardware resetting of the CPU and returning all of its registers to the power-on state.

The SYS_RESETn signal is routed to the pin 35 of the P2 baseboard connector. Refer to the Table 2 for details.

3.14 Boot mode selection

uSomIQ is able to boot in two scenarios:

1) LCD_DATA2 (SYS_BOOT2) is floating
   - NAND
   - NAND I2C
   - MMC0
   - UART0
2) LCD_DATA2 (SYS_BOOT2) is pulled high to 3.3V (a designer **must** use the 3.3V output from uSomIQ)
   - MMC0
   - SPI0
   - UART0
   - USB0

For details check the section 26.1.5 of the AM335x Sitara™ Processors TRM (spruh73 document).

There are 16 pins that control the boot mode of the processor. These pins are shared with LCD pins of the processor. Diagram 9 shows how the boot pins are arranged.

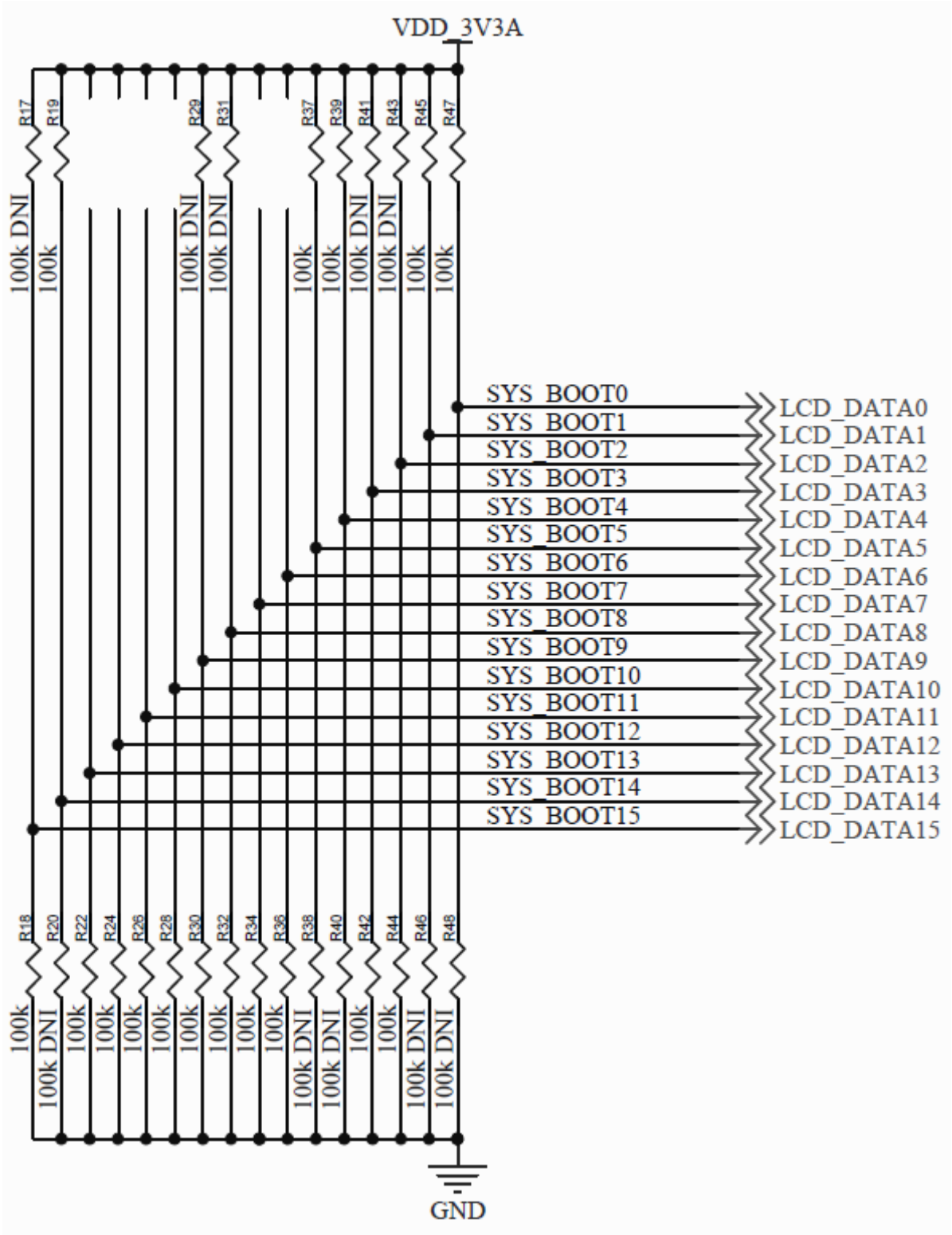

Diagram 12. Boot mode selection.

Table 1 shows the two scenarios set by resistors on the uSomIQ:

Table 1. SYSBOOT Configuration Pins

SYS.BOOT[..]	5	4	3	2	1	0	Boot sequence
Sys_boot[2]=0	1	1	0	0	1	1	NAND-MMC0-UART0 (default)
Sys_boot[2]=1	1	1	0	1	1	1	MMC0-SPI0-UART0-USB0

You can change the default boot sequence by adding, for example, a button to LCD_DATA2 (SYSBOOT2) line which will pull this line to VCC_IO. Figure 10 shows :

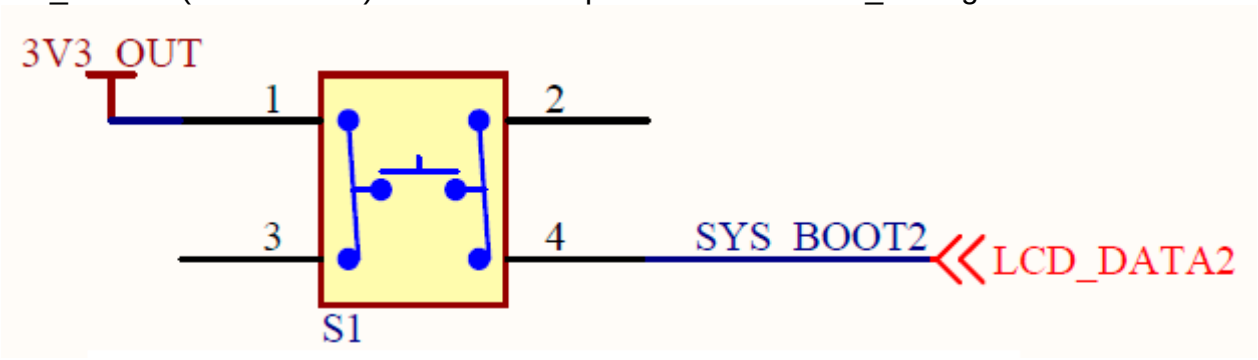

Diagram 13. Boot mode changing schematic.

To change the boot scenario you need to apply the main 5VDC power to uSomIQ while holding the SYS_BOOT2 line in high state. Resetting of AM335x does not change the boot sequence.

If you plan to use any of these signals, then on power up, these pins should not be driven. If you do, it can affect the boot mode of the processor and could keep the processor from booting or working correctly.

3.15 ETHERNET

uSomIQ has 10/100 Ethernet Physical Layer Transceiver SMSC/Microchip LAN8710A installed. LAN8710A supports HP Auto-MDIX technology which means either a straight or a swap cable can be used and this connection is detected automatically. Diagram 11 shows physical connection between the PHY and the CPU. The PHY's RST (reset) line is connected to the global reset signal (SYS_RESETn) issued by the CPU.

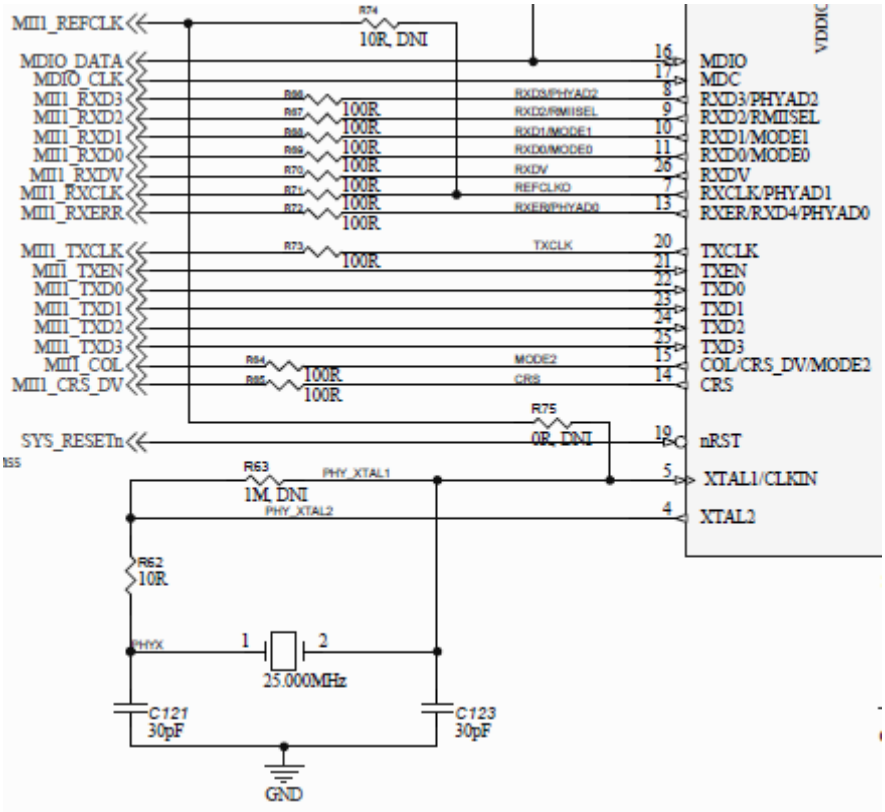

Diagram 14. Ethernet PHY SMSC LAN8710A connection to CPU.

3.16 EEPROM

Some configurations of uSomIQ may hold an EEPROM IC which can be used to identify the board between different software configurations. Basically uSomIQ does not have this IC because this option adds cost but does not mean a lot since users usually build custom software where any HW deviations can be considered.

For software compatibility between different platforms using the same software package the Microchip 24LC32A IC can be installed on uSomIQ. This IC has 32 kB of memory where a device ID can be placed. For device identification between general am335x platforms the following structure description is used in software:

```
struct am335x_evm_eeprom_config {
        u32     header;
        u8      name[8];
        char    version[4];
        u8      serial[12];
        u8      opt[32];
};
```

Where fields are:

- 32 bit header is the same 0xAA5533EE for all AM335x platforms
- name is an ASCII array, “A335USOM” is the uSomIQ identifier.
- version, serial, opt – means only for Beaglebone and TI EVM devices

First 12 bytes are necessary for identification but the others can be ignored. If EEPROM is erased or contains some random values uSomIQ may stop booting.

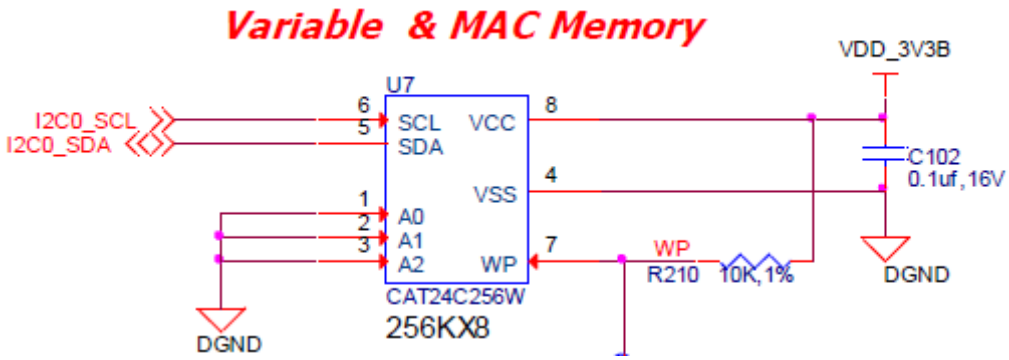

Diagram 15. uSomIQ EEPROM connection.

3.17 Differences between uSomIQ ver.4 and ver.5

Both ver.4 and ver.5 has absolutely the same schematics, architecture and connection except for the single feature: ver.5 can't be powered by USB cable. Ver.4 had this nice feature to be powered from a PC USB port.

This feature was introduced by the original BeagleBone Black schematic and we thought it was nice to power boards from a PC USB port. However this opportunity brought more problems rather than benefits, because the modules had random reboots and still, although a lot of fixes were added to Linux kernel, this problem was not solved. For some hardware assemblies we used the zero Ohm resistor to pull down the USB0_VBUS line, but then the rev.5 was created where we simply disconnected the USB0_VBUS line from the USB power input at TPS65217. The random reboot issue has gone forever. However for simplicity we modified the BoneCape design to power the baseboard by the PC USB port. This modification means nothing for any robust industrial design because such systems are usually powered by highly stabilized power source.

4 Baseboard connectors in details

Tables **2** and **3** hold full description of all signals routed to baseboard connector.

These tables also identify other important terminal characteristics:

- PI – power-in (external power supply)
- PO – power-out (a user can use this source)
- PWR – usually Ground
- I – input
- O – output
- AI – analog input
- AO – analog output
- OD – Open Drain
- Z – high impedance state during reset
- H – high voltage level during reset
- L – low voltage level during reset

Table 2. P2 baseboard connector

Pin #	Pin name	Ball #	Signal name	Mode	Type	Reset state	I/O level
1	5VDC		Main power supply input		PI		
2	GND		Ground		PWR		
3	5VDC		Main power supply input		PI		
4	GND		Ground		PWR		
5	3VDC OUT		3.3V output		PO		
6	1.8VDC OUT		1.8V output (ADC)		PO		
7	3VDC OUT		3.3V output		PO		
8	PB_IN TPS65217		active-low push-button monitor		I		
9	I2C0 SDA		i2c0_sda	0	I/OD		
10	ANALOG GND		Analog Ground for ADC		PWR		
11	I2C0 SCL		i2c0_scl	0	I/OD		
12	ADC IN0	B6	AIN0	0	AI	Z	1.8V
13	MCASP0_AXR1	D13	mcasp0_axr1	0	I/O	L	3.3V
			eQEP0_index	1	I/O		
			mcasp1_axr0	3	I/O		
			EMU3	4	I/O		
			pr1_pru0_pru_r30_6	5	O		
			pr1_pru0_pru_r31_6	6	I		
			gpio3_20	7	I/O		
14	ADC IN1	C7	AIN1	0	AI	Z	1.8V
15	MCASP0_ FSR	C13	mcasp0_fsr	0	I/O	L	3.3V
			eQEP0B_in	1	I		
			mcasp0_axr3	2	I/O		
			mcasp1_fsx	3	I/O		
			EMU2	4	I/O		
			pr1_pru0_pru_r30_5	5	O		
			pr1_pru0_pru_r31_5	6	I		
			gpio3_19	7	I/O		
16	ADC IN2	B7	AIN2	0	AI	Z	1.8V
17	MCASP0_ACLKR	B12	mcasp0_aclkr	0	I/O	L	3.3V
			eQEP0A_in	1	I		
			mcasp0_axr2	2	I/O		
			mcasp1_aclkx	3	I/O		
			mmc0_sdwp	4	I		
			pr1_pru0_pru_r30_4	5	O		
			pr1_pru0_pru_r31_4	6	I		
			gpio3_18	7	I/O		
18	ADC IN3	A7	AIN3	0	AI	Z	1.8V
19	MCASP0_AHCLKR	C12	mcasp0_ahclkr	0	I/O	L	3.3V
			ehrpwm0_synci	1	I		
			mcasp0_axr2	2	I/O		
			spi1_cs0	3	I/O		
			eCAP2_in_PWM2_out	4	I/O		
			pr1_pru0_pru_r30_3	5	O		
			pr1_pru0_pru_r31_3	6	I		
			gpio3_17	7	I/O		
20	ADC IN4	C8	AIN4	0	AI	Z	1.8V

Table 2. P2 baseboard connector (continues)

Pin #	Pin name	Ball #	Signal name	Mode	Type	Reset state	I/O level
21	MCASP0_AXR0	D12	mcasp0_axr0	0	I/O	L	3.3V
			ehrpwm0_tripzone_input	1	I		
			spi1_d1	3	I/O		
			mmc2_sdcd	4	I		
			pr1_pru0_pru_r30_2	5	O		
			pr1_pru0_pru_r31_2	6	I		
			gpio3_16	7	I/O		
22	ADC IN5	B8	AIN5	0	AI	Z	1.8V
23	MCASP0_FSX		mcasp0_fsx	0	I/O	L	3.3V
			ehrpwm0B	1	O		
			spi1_d0	3	I/O		
			mmc1_sdcd	4	I		
			pr1_pru0_pru_r30_1	5	O		
			pr1_pru0_pru_r31_1	6	I		
			gpio3_15	7	I/O		
24	ADC IN6	A8	AIN6	0	AI	Z	1.8V
25	MCASP0_AHCLKX	A14	mcasp0_ahclkx	0	I/O	L	3.3V
			eQEP0_strobe	1	I/O		
			mcasp0_axr3	2	I/O		
			mcasp1_axr1	3	I/O		
			EMU4	4	I/O		
			pr1_pru0_pru_r30_7	5	O		
			pr1_pru0_pru_r31_7	6	I		
			gpio3_21	7	I/O		
26	ADC IN7	C9	AIN7	0	AI	Z	1.8V
27	MCASP0_ACLKX	A13	mcasp0_aclkx	0	I/O	L	3.3V
			ehrpwm0A	1	O		
			spi1_sclk	3	I/O		
			mmc0_sdcd	4	I		
			pr1_pru0_pru_r30_0	5	O		
			pr1_pru0_pru_r31_0	6	I		
			gpio3_14	7	I/O		
28	ANALOG GND				Power		
29	BAT_IN		TPS65217 BAT_IN				
30	UART0 RX	E15	uart0_rxd	0	I	Z	3.3V
			spi1_cs0	1	I/O		
			dcan0_tx	2	O		
			I2C2_SDA	3	I/OD		
			eCAP2_in_PWM2_out	4	I/O		
			pr1_pru1_pru_r30_14	5	O		
			pr1_pru1_pru_r31_14	6	I		
			gpio1_10	7	I/O		
31	BAT_SENSE		TPS65217 BAT_SENSE				

Table 2. P2 baseboard connector (continues)

Pin #	Pin name	Ball #	Signal name	Mode	Type	Reset state	I/O level
32	UART0 TX	E16	uart0_txd	0	O	Z	3.3V
			spi1_cs1	1	I/O		
			dcan0_rx	2	I		
			I2C2_SCL	3	I/OD		
			eCAP1_in_PWM1_out	4	I/O		
			pr1_pru1_pru_r30_15	5	O		
			pr1_pru1_pru_r31_15	6	I		
			gpio1_11	7	I/O		
33	BAT_TS		TPS65217 BAT_TS				
34	UART1 RTS	D17	uart1_rtsn	0	O	Z	3.3V
			timer5	1	I/O		
			dcan0_rx	2	I		
			I2C2_SCL	3	I/OD		
			spi1_cs1	4	I/O		
			pr1_uart0_rts_n	5	O		
			pr1_edc_latch1_in	6	I		
			gpio0_13	7	I/O		
35	SYS_RESETN	A10	nRESETIN_OUT	0	I/OD	0	3.3V
36	UART1 CTS	D18	uart1_ctsn	0	I	Z	3.3V
			timer6	1	I/O		
			dcan0_tx	2	O		
			I2C2_SDA	3	I/OD		
			spi1_cs0	4	I/O		
			pr1_uart0_cts_n	5	I		
			pr1_edc_latch0_in	6	I		
			gpio0_12	7	I/O		
37	GPIO0_20	D14	xdma_event_intr1	0	I	Z	3.3V
			tclkin	2	I		
			clkout2	3	O		
			timer7	4	I/O		
			pr1_pru0_pru_r31_16	5	I		
			EMU3	6	I/O		
			gpio0_20	7	I/O		
38	UART1 RX	D16	uart1_rxd	0	I	Z	3.3V
			mmc1_sdwp	1	I		
			dcan1_tx	2	O		
			I2C1_SDA	3	I/OD		
			pr1_uart0_rxd	5	I		
			pr1_pru1_pru_r31_16	6	I		
			gpio0_14	7	I/O		
39	GPIO0_19	A15	xdma_event_intr0	0	I	Z	3.3V
			timer4	2	I/O		
			clkout1	3	O		
			spi1_cs1	4	I/O		
			pr1_pru1_pru_r31_16	5	I		
			EMU2	6	I/O		
			gpio0_19	7	I/O		

Table 2. P2 baseboard connector (continues)

Pin #	Pin name	Ball #	Signal name	Mode	Type	Reset state	I/O level
40	UART1 TX	D15	uart1_txd	0	O	Z	3.3V
			mmc2_sdwp	1	I		
			dcan1_rx	2	I		
			I2C1_SCL	3	I/OD		
			pr1_uart0_txd	5	O		
			pr1_pru0_pru_r31_16	6	I		
			gpio0_15	7	I/O		
41	GND				PWR		
42	UART3 RX	C15	spi0_cs1	0	I/O	Z	3.3V
			uart3_rxd	1	I		
			eCAP1_in_PWM1_out	2	I/O		
			mmc0_pow	3	O		
			xdma_event_intr2	4	I		
			mmc0_sdcd	5	I		
			EMU4	6	I/O		
			gpio0_6	7	I/O		
43	DCAN1 RX	E17	uart0_rtsn	0	O	Z	3.3V
			uart4_txd	1	O		
			dcan1_rx	2	I		
			I2C1_SCL	3	I/OD		
			spi1_d1	4	I/O		
			spi1_cs0	5	I/O		
			pr1_edc_sync1_out	6	O		
			gpio1_9	7	I/O		
44	UART3 TX	C18	eCAP0_in_PWM0_out	0	I/O	Z	3.3V
			uart3_txd	1	O		
			spi1_cs1	2	I/O		
			pr1_ecap0_ecap_capin_apwm_o	3	I/O		
			spi1_sclk	4	I/O		
			mmc0_sdwp	5	I		
			xdma_event_intr2	6	I		
			gpio0_7	7	I/O		
45	DCAN1 TX	E18	uart0_ctsn	0	I	Z	3.3V
			uart4_rxd	1	I		
			dcan1_tx	2	O		
			I2C1_SDA	3	I/OD		
			spi1_d0	4	I/O		
			timer7	5	I/O		
			pr1_edc_sync0_out	6	O		
			gpio1_8	7	I/O		
46	SPI0_D1	B16	spi0_d1	0	I/O	Z	3.3V
			mmc1_sdwp	1	I		
			I2C1_SDA	2	I/OD		
			ehrpwm0_tripzone_input	3	I		
			pr1_uart0_rxd	4	I		
			pr1_edio_data_in0	5	I		
			pr1_edio_data_out0	6	O		
			gpio0_4	7	I/O		

Table 2. P2 baseboard connector (continues)

Pin #	Pin name	Ball #	Signal name	Mode	Type	Reset state	I/O level
47	MMC0 DATA3	F17	mmc0_dat3	0	I/O	Z	3.3V
			gpmc_a20	1	O		
			uart4_ctsn	2	I		
			timer5	3	I/O		
			uart1_dcdn	4	I		
			pr1_pru0_pru_r30_8	5	O		
			pr1_pru0_pru_r31_8	6	I		
			gpio2_26	7	I/O		
48	SPI0_D0	B17	spi0_d0	0	I/O	Z	3.3V
			uart2_txd	1	O		
			I2C2_SCL	2	I/OD		
			ehrpwm0B	3	O		
			pr1_uart0_rts_n	4	O		
			pr1_edio_latch_in	5	I		
			EMU3	6	I/O		
			gpio0_3	7	I/O		
49	MMC0 DATA2	F18	mmc0_dat2	0	I/O	H	3.3V
			gpmc_a21	1	O		
			uart4_rtsn	2	O		
			timer6	3	I/O		
			uart1_dsrn	4	I		
			pr1_pru0_pru_r30_9	5	O		
			pr1_pru0_pru_r31_9	6	I		
			gpio2_27	7	I/O		
50	SPI0 SCLK	A17	spi0_sclk	0	I/O	Z	3.3V
			uart2_rxd	1	I		
			I2C2_SDA	2	I/OD		
			ehrpwm0A	3	O		
			pr1_uart0_cts_n	4	I		
			pr1_edio_sof	5	O		
			EMU2	6	I/O		
			gpio0_2	7	I/O		
51	MMC0 DATA1	G15	mmc0_dat1	0	I/O	H	3.3V
			gpmc_a22	1	O		
			uart5_ctsn	2	I		
			uart3_rxd	3	I		
			uart1_dtrn	4	O		
			pr1_pru0_pru_r30_10	5	O		
			pr1_pru0_pru_r31_10	6	I		
			gpio2_28	7	I/O		
52	SPI0 CS0	A16	spi0_cs0	0	I/O	Z	3.3V
			mmc2_sdwp	1	I		
			I2C1_SCL	2	I/OD		
			ehrpwm0_synci	3	I		
			pr1_uart0_txd	4	O		
			pr1_edio_data_in1	5	I		
			pr1_edio_data_out1	6	O		
			gpio0_5	7	I/O		

Table 2. P2 baseboard connector (continues)

Pin #	Pin name	Ball #	Signal name	Mode	Type	Reset state	I/O level
53	MMC0 DATA0	G16	mmc0_dat0	0	I/O	H	3.3V
			gpmc_a23	1	O		
			uart5_rtsn	2	O		
			uart3_txd	3	O		
			uart1_rin	4	I		
			pr1_pru0_pru_r30_11	5	O		
			pr1_pru0_pru_r31_11	6	I		
			gpio2_29	7	I/O		
54	USB0 VBUS	P15	USB0_VBUS	0	A	Z	5V
55	MMC0 CMD	G18	mmc0_cmd	0	I/O	H	3.3V
			gpmc_a25	1	O		
			uart3_rtsn	2	O		
			uart2_txd	3	O		
			dcan1_rx	4	I		
			pr1_pru0_pru_r30_13	5	O		
			pr1_pru0_pru_r31_13	6	I		
			gpio2_31	7	I/O		
56	USB0 DRVBUS	F16	USB0_DRVVBUS	0	O	L	3.3V
			gpio0_18	7	I/O		
57	MMC0 CLKO	G17	mmc0_clk	0	I/O	H	3.3V
			gpmc_a24	1	O		
			uart3_ctsn	2	I		
			uart2_rxd	3	I		
			dcan1_tx	4	O		
			pr1_pru0_pru_r30_12	5	O		
			pr1_pru0_pru_r31_12	6	I		
			gpio2_30	7	I/O		
58	USB0 ID	P16	USB0_ID	0	A	Z	3.3V
59	GND		Ground		PWR		
60	GND		Ground				
61	ETH RX+		Ethernet Receive Positive				
62	USB0+		USB0 DATA POSITIVE	0	A	Z	3.3VA
63	ETH RX-		Ethernet Receive Negative				
64	USB0-		USB0 DATA NEGATIVE	0	A	Z	3.3VA
65	GND		Ground		PWR		
66	GND		Ground		PWR		
67	ETH TX+		Ethernet Transmit Positive				
68	ETH LED 100Mb		Ethernet LED 100Mb				
69	ETH RX-		Ethernet Transmit Negative				
70	ETH ACTIVE LED		Ethernet LED Activity				

Table 3. P3 baseboard connector

Pin #	Pin name	Ball #	Signal name	Mode	Type	Reset state	I/O level
1	LCD DATA4	T1	lcd_data4	0	I/O	Z	3.3V
			gpmc_a4	1	O		
			pr1_mii0_txd1	2	O		
			eQEP2A_in	3	I		
			pr1_pru1_pru_r30_4	5	O		
			pr1_pru1_pru_r31_4	6	I		
			gpio2_10	7	I/O		
2	LCD DATA6	T3	lcd_data6	0	I/O	Z	3.3V
			gpmc_a6	1	O		
			pr1_edio_data_in6	2	I		
			eQEP2_index	3	I/O		
			pr1_edio_data_out6	4	O		
			pr1_pru1_pru_r30_6	5	O		
			pr1_pru1_pru_r31_6	6	I		
			gpio2_12	7	I/O		
3	LCD DATA5	T2	lcd_data5	0	I/O	Z	3.3V
			gpmc_a5	1	O		
			pr1_mii0_txd0	2	O		
			eQEP2B_in	3	I		
			pr1_pru1_pru_r30_5	5	O		
			pr1_pru1_pru_r31_5	6	I		
			gpio2_11	7	I/O		
4	LCD DATA7	T4	lcd_data7	0	I/O	Z	3.3V
			gpmc_a7	1	O		
			pr1_edio_data_in7	2	I		
			eQEP2_strobe	3	I/O		
			pr1_edio_data_out7	4	O		
			pr1_pru1_pru_r30_7	5	O		
			pr1_pru1_pru_r31_7	6	I		
			gpio2_13	7	I/O		
5	LCD DATA3	R4	lcd_data3	0	I/O	Z	3.3V
			gpmc_a3	1	O		
			pr1_mii0_txd2	2	O		
			ehrpwm0_synco	3	O		
			pr1_pru1_pru_r30_3	5	O		
			pr1_pru1_pru_r31_3	6	I		
			gpio2_9	7	I/O		
6	LCD DATA8	U1	lcd_data8	0	I/O	Z	3.3V
			gpmc_a12	1	O		
			ehrpwm1_tripzone_input	2	I		
			mcasp0_aclkx	3	I/O		
			uart5_txd	4	O		
			pr1_mii0_rxd3	5	I		
			uart2_ctsn	6	I		
			gpio2_14	7	I/O		
7	LCD DATA2	R3	lcd_data2	0	I/O	Z	3.3V
			gpmc_a2	1	O		
			pr1_mii0_txd3	2	O		
			ehrpwm2_tripzone_input	3	I		
			pr1_pru1_pru_r30_2	4	O		
			pr1_pru1_pru_r31_2	5	I		
			gpio2_8	6	I/O		

Table 3. P3 baseboard connector (continues)

Pin #	Pin name	Ball #	Signal name	Mode	Type	Reset state	I/O level
8	LCD DATA9	U2	lcd_data9	0	I/O	Z	3.3V
			gpmc_a13	1	O		
			ehrpwm0_synco	2	O		
			mcasp0_fsx	3	I/O		
			uart5_rxd	4	I		
			pr1_mii0_rxd2	5	I		
			uart2_rtsn	6	O		
			gpio2_15	7	I/O		
9	LCD DATA1	R2	lcd_data1	0	I/O	Z	3.3V
			gpmc_a1	1	O		
			pr1_mii0_txen	2	O		
			ehrpwm2B	3	O		
			pr1_pru1_pru_r30_1	5	O		
			pr1_pru1_pru_r31_1	6	I		
			gpio2_7	7	I/O		
10	LCD DATA10	U3	lcd_data10	0	I/O	Z	3.3V
			gpmc_a14	1	O		
			ehrpwm1A	2	O		
			mcasp0_axr0	3	I/O		
			pr1_mii0_rxd1	5	I		
			uart3_ctsn	6	I		
			gpio2_16	7	I/O		
11	LCD DATA0	R1	lcd_data0	0	I/O	Z	3.3V
			gpmc_a0	1	O		
			pr1_mii_mt0_clk	2	I		
			ehrpwm2A	3	O		
			pr1_pru1_pru_r30_0	5	O		
			pr1_pru1_pru_r31_0	6	I		
			gpio2_6	7	I/O		
12	LCD DATA11	U4	lcd_data11	0	I/O	Z	3.3V
			gpmc_a15	1	O		
			ehrpwm1B	2	O		
			mcasp0_ahclkr	3	I/O		
			mcasp0_axr2	4	I/O		
			pr1_mii0_rxd0	5	I		
			uart3_rtsn	6	O		
			gpio2_17	7	I/O		
13	LCD Data Enable	R6	lcd_ac_bias_en	0	O	Z	3.3V
			gpmc_a11	1	O		
			pr1_mii1_crs	2	I		
			pr1_edio_data_in5	3	I		
			pr1_edio_data_out5	4	O		
			pr1_pru1_pru_r30_11	5	O		
			pr1_pru1_pru_r31_11	6	I		
			gpio2_25	7	I/O		

Table 3. P3 baseboard connector (continues)

Pin #	Pin name	Ball #	Signal name	Mode	Type	Reset state	I/O level
14	LCD DATA12	V2	lcd_data12	0	I/O	Z	3.3V
			gpmc_a16	1	O		
			eQEP1A_in	2	I		
			mcasp0_aclkr	3	I/O		
			mcasp0_axr2	4	I/O		
			pr1_mii0_rxlink	5	I		
			uart4_ctsn	6	I		
			gpio0_8	7	I/O		
15	LCD HSYNC	R5	lcd_hsync	0	O	Z	3.3V
			gpmc_a9	1	O		
			gpmc_a2	2	O		
			pr1_edio_data_in3	3	I		
			pr1_edio_data_out3	4	O		
			pr1_pru1_pru_r30_9	5	O		
			pr1_pru1_pru_r31_9	6	I		
			gpio2_23	7	I/O		
16	LCD DATA13	V3	lcd_data13	0	I/O	Z	3.3V
			gpmc_a17	1	O		
			eQEP1B_in	2	I		
			mcasp0_fsr	3	I/O		
			mcasp0_axr3	4	I/O		
			pr1_mii0_rxer	5	I		
			uart4_rtsn	6	O		
			gpio0_9	7	I/O		
17	LCD VSYNC	U5	lcd_vsync	0	O	Z	3.3V
			gpmc_a8	1	O		
			gpmc_a1	2	O		
			pr1_edio_data_in2	3	I		
			pr1_edio_data_out2	4	O		
			pr1_pru1_pru_r30_8	5	O		
			pr1_pru1_pru_r31_8	6	I		
			gpio2_22	7	I/O		
18	LCD DATA14	V4	lcd_data14	0	I/O	Z	3.3V
			gpmc_a18	1	O		
			eQEP1_index	2	I/O		
			mcasp0_axr1	3	I/O		
			uart5_rxd	4	I		
			pr1_mii_mr0_clk	5	I		
			uart5_ctsn	6	I		
			gpio0_10	7	I/O		
19	LCD PCLK	V5	lcd_pclk	0	O	Z	3.3V
			gpmc_a10	1	O		
			pr1_mii0_crs	2	I		
			pr1_edio_data_in4	3	I		
			pr1_edio_data_out4	4	O		
			pr1_pru1_pru_r30_10	5	O		
			pr1_pru1_pru_r31_10	6	I		
			gpio2_24	7	I/O		

Table 3. P3 baseboard connector (continues)

Pin #	Pin name	Ball #	Signal name	Mode	Type	Reset state	I/O level
20	LCD DATA15	T5	lcd_data15	0	I/O	Z	3.3V
			gpmc_a19	1	O		
			eQEP1_strobe	2	I/O		
			mcasp0_ahclkx	3	I/O		
			mcasp0_axr3	4	I/O		
			pr1_mii0_rxdv	5	I		
			uart5_rtsn	6	O		
			gpio0_11	7	I/O		
21	GND				PWR		
22	GND				PWR		
23	GPMC AD0	U7	gpmc_ad0	0	I/O	L	3.3V
			mmc1_dat0	1	I/O		
			gpio1_0	7	I/O		
24	GPMC ALE	R7	gpmc_advn_ale	0	O	H	3.3V
			timer4	2	I/O		
			gpio2_2	7	I/O		
25	GPMC AD1		gpmc_ad1	0	I/O	L	3.3V
			mmc1_dat1	1	I/O		
			gpio1_1	7	I/O		
26	GPMC OE	T7	gpmc_oen_ren	0	O	H	3.3V
			timer7	2	I/O		
			gpio2_3	7	I/O		
27	GPMC AD2	R8	gpmc_ad2	0	I/O	L	3.3V
			mmc1_dat2	1	I/O		
			gpio1_2	7	I/O		
28	GPMC CS0	V6	gpmc_csn0	0	O	H	3.3V
			gpio1_29	7	I/O		
29	GPMC AD3	T8	gpmc_ad3	0	I/O	L	3.3V
			mmc1_dat3	1	I/O		
			gpio1_3	7	I/O		
30	GPMC WE	U6	gpmc_wen	0	O	H	3.3V
			timer6	2	I/O		
			gpio2_4	7	I/O		
31	GPMC AD4	U8	gpmc_ad4	0	I/O	L	3.3V
			mmc1_dat4	1	I/O		
			gpio1_4	7	I/O		
32	GPMC CLE	R7	gpmc_advn_ale	0	O	H	3.3V
			timer4	2	I/O		
			gpio2_2	7	I/O		
33	GPMC AD5	V8	gpmc_ad5	0	I/O	L	3.3V
			mmc1_dat5	1	I/O		
			gpio1_5	7	I/O		
34	GPMC CS3	T13	gpmc_csn3	0	O	H	3.3V
			gpmc_a3	1	O		
			rmii2_crs_dv	2	I		
			mmc2_cmd	3	I/O		
			pr1_mii0_crs	4	I		
			pr1_mdio_data	5	I/O		
			EMU4	6	I/O		
			gpio2_0	7	I/O		

Table 3. P3 baseboard connector (continues)

Pin #	Pin name	Ball #	Signal name	Mode	Type	Reset state	I/O level
35	GPMC AD6	R9	gpmc_ad6	0	I/O	L	3.3V
			mmc1_dat6	1	I/O		
			gpio1_6	7	I/O		
36	GPMC CS2	V9	gpmc_csn2	0	O	H	3.3V
			gpmc_be1n	1	O		
			mmc1_cmd	2	I/O		
			pr1_edio_data_in7	3	I		
			pr1_edio_data_out7	4	O		
			pr1_pru1_pru_r30_13	5	O		
			pr1_pru1_pru_r31_13	6	I		
			gpio1_31	7	I/O		
37	GPMC AD7	T9	gpmc_ad7	0	I/O	L	3.3V
			mmc1_dat7	1	I/O		
			gpio1_7	7	I/O		
38	GPMC CS1	U9	gpmc_csn1	0	O	H	3.3V
			gpmc_clk	1	I/O		
			mmc1_clk	2	I/O		
			pr1_edio_data_in6	3	I		
			pr1_edio_data_out6	4	O		
			pr1_pru1_pru_r30_12	5	O		
			pr1_pru1_pru_r31_12	6	I		
			gpio1_30	7	I/O		
39	GPMC AD8	U10	gpmc_ad8	0	I/O	L	3.3V
			lcd_data23	1	O		
			mmc1_dat0	2	I/O		
			mmc2_dat4	3	I/O		
			ehrpwm2A	4	O		
			pr1_mii_mt0_clk	5	I		
			gpio0_22	7	I/O		
40	GPMC CLK	V12	gpmc_clk	0	I/O	L	3.3V
			lcd_memory_clk	1	O		
			gpmc_wait1	2	I		
			mmc2_clk	3	I/O		
			pr1_mii1_crs	4	I		
			pr1_mdio_mdclk	5	O		
			mcasp0_fsr	6	I/O		
			gpio2_1	7	I/O		
41	GPMC AD9	T10	gpmc_ad9	0	I/O	L	3.3V
			lcd_data22	1	O		
			mmc1_dat1	2	I/O		
			mmc2_dat5	3	I/O		
			ehrpwm2B	4	O		
			pr1_mii0_col	5	I		
			gpio0_23	7	I/O		
42	GPMC AD11	U12	gpmc_ad11	0	I/O	L	3.3V
			lcd_data20	1	O		
			mmc1_dat3	2	I/O		
			mmc2_dat7	3	I/O		
			ehrpwm0_synco	4	O		
			pr1_mii0_txd3	5	O		
			gpio0_27	7	I/O		

Table 3. P3 baseboard connector (continues)

Pin #	Pin name	Ball #	Signal name	Mode	Type	Reset state	I/O level
43	GPMC AD10	T11	gpmc_ad10	0	I/O	L	3.3V
			lcd_data21	1	O		
			mmc1_dat2	2	I/O		
			mmc2_dat6	3	I/O		
			ehrpwm2_tripzone_input	4	I		
			pr1_mii0_txen	5	O		
			gpio0_26	7	I/O		
44	GPMC AD12	T12	gpmc_ad12	0	I/O	L	3.3V
			lcd_data19	1	O		
			mmc1_dat4	2	I/O		
			mmc2_dat0	3	I/O		
			eQEP2A_in	4	I		
			pr1_mii0_txd2	5	O		
			pr1_pru0_pru_r30_14	6	O		
			gpio1_12	7	I/O		
45	GPMC AD14	V13	gpmc_ad14	0	I/O	L	3.3V
			lcd_data17	1	O		
			mmc1_dat6	2	I/O		
			mmc2_dat2	3	I/O		
			eQEP2_index	4	I/O		
			pr1_mii0_txd0	5	O		
			pr1_pru0_pru_r31_14	6	I		
			gpio1_14	7	I/O		
46	GPMC AD13	R12	gpmc_ad13	0	I/O	L	3.3V
			lcd_data18	1	O		
			mmc1_dat5	2	I/O		
			mmc2_dat1	3	I/O		
			eQEP2B_in	4	I		
			pr1_mii0_txd1	5	O		
			pr1_pru0_pru_r30_15	6	O		
			gpio1_13	7	I/O		
47	GPMC AD15	U13	gpmc_ad15	0	I/O	L	3.3V
			lcd_data16	1	O		
			mmc1_dat7	2	I/O		
			mmc2_dat3	3	I/O		
			eQEP2_strobe	4	I/O		
			pr1_ecap0_ecap_capin_apwm_o	5	I/O		
			pr1_pru0_pru_r31_15	6	I		
			gpio1_15	7	I/O		
48	GPMC A0	R13	gpmc_a0	0	O	L	3.3V
			gmii2_txen	1	O		
			rgmii2_tctl	2	O		
			rmii2_txen	3	O		
			gpmc_a16	4	O		
			pr1_mii_mt1_clk	5	I		
			ehrpwm1_tripzone_input	6	I		
			gpio1_16	7	I/O		

Table 3. P3 baseboard connector (continues)

Pin #	Pin name	Ball #	Signal name	Mode	Type	Reset state	I/O level
49	GPMC A6	U15	gpmc_a6	0	O	L	3.3V
			gmii2_txclk	1	I		
			rgmii2_tclk	2	O		
			mmc2_dat4	3	I/O		
			gpmc_a22	4	O		
			pr1_mii1_rxd2	5	I		
			eQEP1_index	6	I/O		
			gpio1_22	7	I/O		
50	GPMC A1	V14	gpmc_a1	0	O	L	3.3V
			gmii2_rxdv	1	I		
			rgmii2_rctl	2	I		
			mmc2_dat0	3	I/O		
			gpmc_a17	4	O		
			pr1_mii1_txd3	5	O		
			ehrpwm0_synco	6	O		
			gpio1_17	7	I/O		
51	GPMC A7	T15	gpmc_a7	0	O	L	3.3V
			gmii2_rxclk	1	I		
			rgmii2_rclk	2	I		
			mmc2_dat5	3	I/O		
			gpmc_a23	4	O		
			pr1_mii1_rxd1	5	I		
			eQEP1_strobe	6	I/O		
			gpio1_23	7	I/O		
52	GPMC A2	U14	gpmc_a2	0	O	L	3.3V
			gmii2_txd3	1	O		
			rgmii2_td3	2	O		
			mmc2_dat1	3	I/O		
			gpmc_a18	4	O		
			pr1_mii1_txd2	5	O		
			ehrpwm1A	6	O		
			gpio1_18	7	I/O		
53	GPMC A8	V16	gpmc_a8	0	O	L	3.3V
			gmii2_rxd3	1	I		
			rgmii2_rd3	2	I		
			mmc2_dat6	3	I/O		
			gpmc_a24	4	O		
			pr1_mii1_rxd0	5	I		
			mcasp0_aclkx	6	I/O		
			gpio1_24	7	I/O		
54	GPMC A3	T14	gpmc_a3	0	O	L	3.3V
			gmii2_txd2	1	O		
			rgmii2_td2	2	O		
			mmc2_dat2	3	I/O		
			gpmc_a19	4	O		
			pr1_mii1_txd1	5	O		
			ehrpwm1B	6	O		
			gpio1_19	7	I/O		

Table 3. P3 baseboard connector (continues)

Pin #	Pin name	Ball #	Signal name	Mode	Type	Reset state	I/O level
55	GPMC A9	U16	gpmc_a9	0	O	L	3.3V
			gmii2_rxd2	1	I		
			rgmii2_rd2	2	I		
			mmc2_dat7 / rmii2_crs_dv	3	I/O		
			gpmc_a25	4	O		
			pr1_mii_mr1_clk	5	I		
			mcasp0_fsx	6	I/O		
			gpio1_25	7	I/O		
56	GPMC A4	R14	gpmc_a4	0	O	L	3.3V
			gmii2_txd1	1	O		
			rgmii2_td1	2	O		
			rmii2_txd1	3	O		
			gpmc_a20	4	O		
			pr1_mii1_txd0	5	O		
			eQEP1A_in	6	I		
			gpio1_20	7	I/O		
57	GPMC A10	T16	gpmc_a10	0		L	3.3V
			gmii2_rxd1	1			
			rgmii2_rd1	2			
			rmii2_rxd1	3			
			gpmc_a26	4			
			pr1_mii1_rxdv	5			
			mcasp0_axr0	6			
			gpio1_26	7			
58	GPMC A5	V15	gpmc_a5	0	O	L	3.3V
			gmii2_txd0	1	O		
			rgmii2_td0	2	O		
			rmii2_txd0	3	O		
			gpmc_a21	4	O		
			pr1_mii1_rxd3	5	I		
			eQEP1B_in	6	I		
			gpio1_21	7	I/O		
59	GPMC A11	V17	gpmc_a11	0	O	L	3.3V
			gmii2_rxd0	1	I		
			rgmii2_rd0	2	I		
			rmii2_rxd0	3	I		
			gpmc_a27	4	O		
			pr1_mii1_rxer	5	I		
			mcasp0_axr1	6	I/O		
			gpio1_27	7	I/O		
60	GND		Ground		PWR		
61	GPMC WP	U17	gpmc_wpn	0	O	H	3.3V
			gmii2_rxerr	1	I		
			gpmc_csn5	2	O		
			rmii2_rxerr	3	I		
			mmc2_sdcd	4	I		
			pr1_mii1_txen	5	O		
			uart4_txd	6	O		
			gpio0_31	7	I/O		
62	USB1 VBUS	T18	USB1_VBUS	0		Z	

Table 3. P3 baseboard connector (continues)

Pin #	Pin name	Ball #	Signal name	Mode	Type	Reset state	I/O level
63	GPMC WAIT	T17	gpmc_wait0	0	I	H	3.3V
			gmii2_crs	1	I		
			gpmc_csn4	2	O		
			rmii2_crs_dv	3	I		
			mmc1_sdcd	4	I		
			pr1_mii1_col	5	I		
			uart4_rxd	6	I		
			gpio0_30	7	I/O		
64	USB1 DRVVBUS	F15	USB1 DRVVBUS	0	O	L	3.3V
			gpio3_13	7	I/O		
65	GPMC BE1	U18	gpmc_be1n	0	O	H	3.3V
			gmii2_col	1	I		
			gpmc_csn6	2	O		
			mmc2_dat3	3	I/O		
			gpmc_dir	4	O		
			pr1_mii1_rxlink	5	I		
			mcasp0_aclkr	6	I/O		
			gpio1_28	7	I/O		
66	GND		Ground	0	PWR		
67	MDIO_DATA	M17	MDIO Data	0	IO		3.3V
68	USB1+	R17	USB1_DP	0			
69	MDIO_CLK	M18	MDIO Clock	0	O		3.3V
70	USB1-	R18	USB1_DM	0			

5 Absolute maximum ratings

5.1 ELECTRICAL CHARACTERISTICS

Table 4. Electrical characteristics

Item	Min.	Typ.	Max.	units
Power				
5VDC input	4.3	5	5.5	V
Consumption		400	1000	mA
3.3V output		3.3		V
Possible current load for 3.3V output				
LDO TL5209DR installed			300	mA
LDO TL5209DR not installed			100	mA
1.8V output	1.75	1.8	1.85	V
Possible current load for 1.8V output			50	mA
Voltage levels for I/O				
All GPIO and interfaces		3.3	3.8	V
USB	-0.5		4	V
USB0_VBUS / USB1_VBUS			5.25	V
USB0_ID	-0.5		2.1	V
Ethernet DM/DP			6	V

5.2 Mechanical specification

All units are in millimeters.

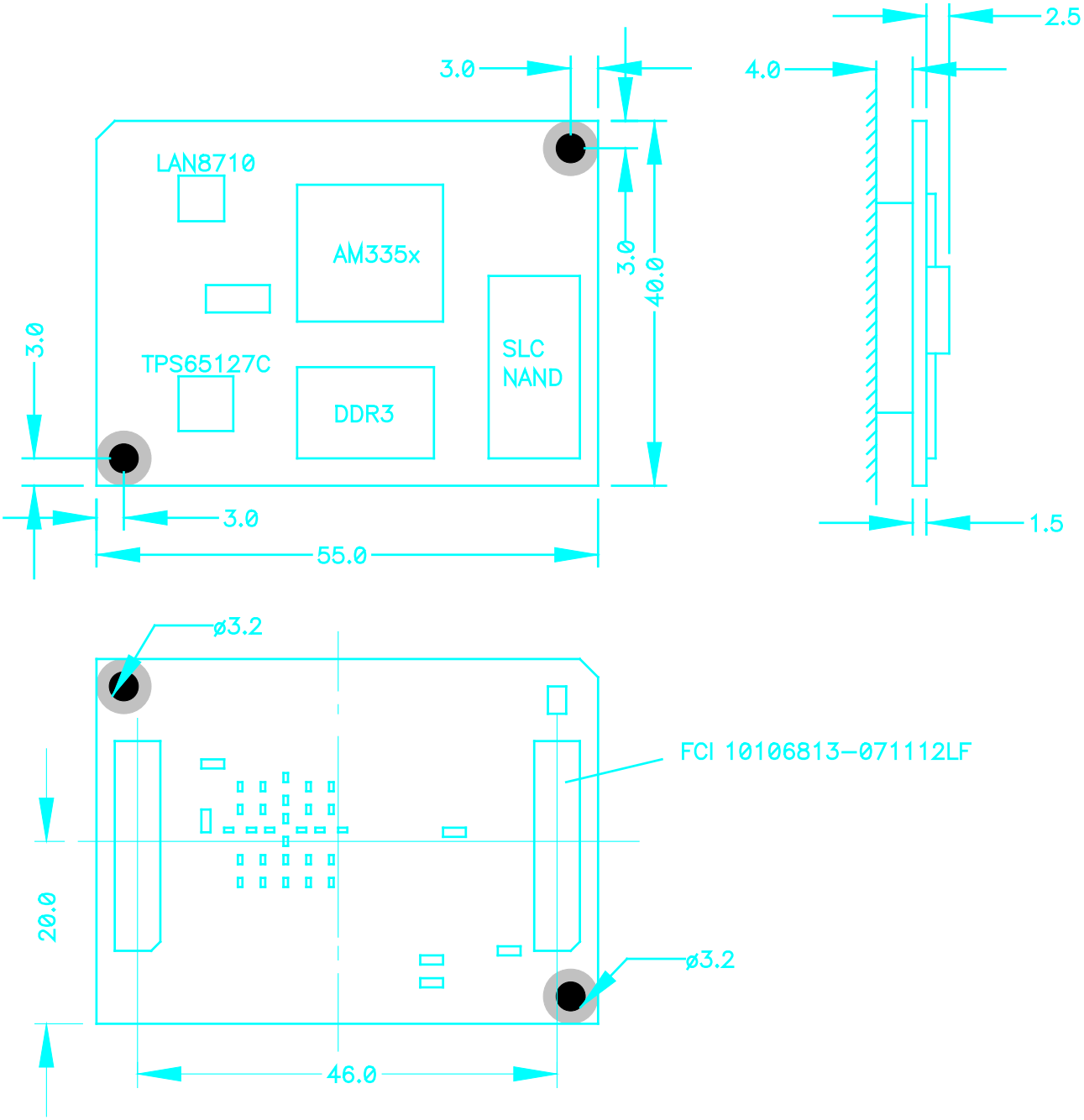

Diagram 16. uSomIQ dimensions.

Table 5. Mechanical properties

Item	Typ	Units
Length	55	mm
Width	40	mm
Thickness (max.)	5.2	mm
Mass	5	gram

5.3 Thermal specification

Table 6. Temperature ratings

Temperature ºC	Min.	Max.
Storage	-40	+85
Working (commercial)	0	70
Working (extended)	-20	+85
Working (industrial)	-40	+85
Humidity %, without condensing	10	70

5.4 Available baseboard connectors

FCI MezzoStak connectors with 70 pins are used on both uSomIQ and a baseboard. MezzoStak is a family of hermaphrodite connectors that means that the same part numbers are used for mating.

The following connector may be used for the baseboard connectivity:

Vendor	Part number
FCI	10106813-071112LF
FCI	10106813-171112LF (not recommended)

6 Document history

Version	Date	Changes Description
b	20.11.2015	New uSomIQ Rev.5 introduced
a	15.09.2014	Initial version